

V1

May 8, 2000

cs470 - Computer Architecture 1
Spring 2000

Final Exam

open books, open notes

Starts: **7:30 pm**Ends: **9:30 pm**

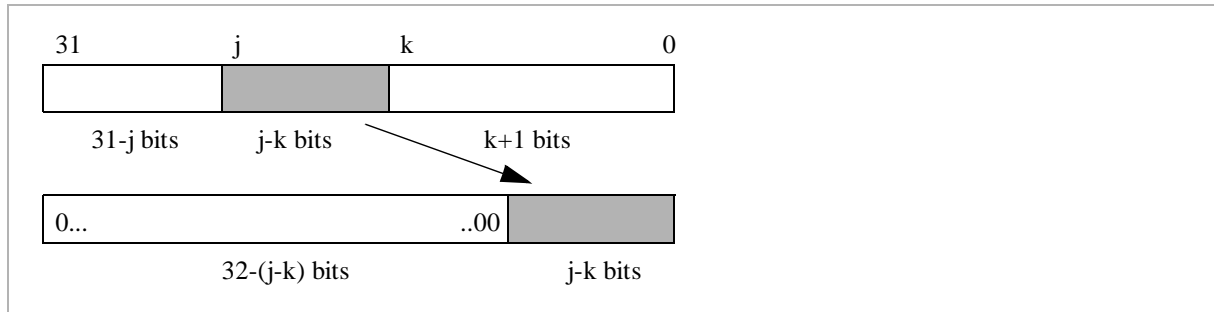
Name: _____ (please print)

ID: _____

Problem	Max points	Your mark	Comments
1	20		5+5+10
2	55		10+10+5+5+5+5+5+5+5
3	15		
4	10		
	100		

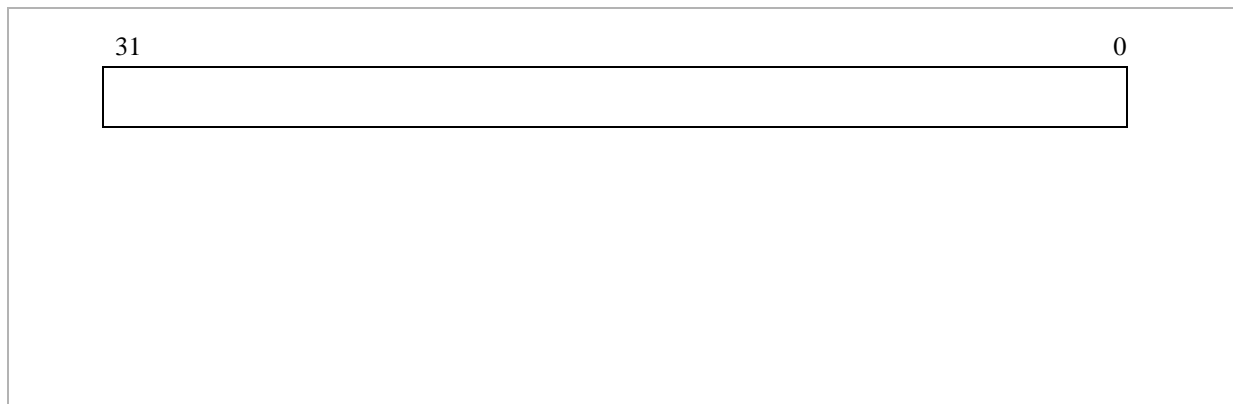
What happens with this paper (mark one): **Discard** **Mail** at the following address:

1. Some computers have explicit instructions to extract an arbitrary field from a 32-bit register and place it in the least significant bits of a register. The operation is depicted below:



- a) Find the shortest sequence of MIPS native instructions that extracts a field, assuming that $k=8$, $j=17$, the field is extracted from register $\$t1$ and the result is stored in register $\$t0$.

- b) Assume that we want to introduce such an instruction in the MIPS instruction set. Indicate a possible format for this instruction.



- c) What extra hardware resources would be needed to support this instruction on the single clock cycle datapath MIPS (figure 5.19 at page 360)? Use the attached sheet to show your solution.

Address (in hexadecimal)	Cache Hit or Miss	TLB Hit or Miss	Page Faults

b) Assume a direct mapped cache with a size of 32 bytes, with 4 bytes per block and a write-back policy. Assume that all the blocks in the cache are invalid at the time the program starts executing. Show the contents of the cache after the last statement has been executed. Make sure to label each reference as a hit or miss in the 'Cache Hit or Miss' column of the above table. Use the ruled page attached to this exam to show the cache. Clearly mark the limits of your cache and label the fields of it.

c) What is the miss-rate?

d) The system on which you run the program has virtual memory, with a page size of 2 KB and a main memory of 32 MB. Show the size of various fields in the virtual address.

e) What is the size of the page table? Assume that each entry in the table has a size which is a multiple of byte; each entry uses four bits for various purposes ('Valid', 'Dirty', etc.).

f) What is the contents of the variable `var2` after the program executes? Assume a Big Endian memory model.

3. Consider a program consisting of 100

```
lw $8, 0($8)
```

instructions (don't worry about whether this code is any good). What would the actual CPI be if the program were run on the pipelined datapath on Figure 6.45 on page 491?

4. You have a register-register architecture that has two addressing modes, base-displacement and memory indirect, besides register and immediate. You want to improve this architecture by eliminating the memory indirect addressing mode: this will decrease the clock cycle by 10% but will increase somehow the instruction count because you will have to replace instructions like:

```
lw R1, @(R2)
```

with a sequence of instructions. Assume that the frequency of memory indirect addressing

is 5%, and that the overall CPI does not change.

a) show the sequence of instructions that will replace every memory indirect addressing;

b) how does the performance of the new architecture compare with the performance of the original?

