CONTENTS

1. F	Fundamentals of Computer Design	3
	1.1 Introduction	
	1.2 Performance definition	
	1.3 What drives the work of a computer designer.	8
	1.3.1 Qualitative aspects of design	
	1.3.2 Quantitative aspects.	
2 [Paria Organization of a Commutan	10
Z. I	Basic Organization of a Computer.	
	2.1 The block diagram	
	2.2 Computation and control in CPU.	
	2.3 Instruction cycle	23
3. I	Instruction Set Design	
	3.1 RISC/CISC, where is the difference	29
	3.2 How many addresses?	32
	3.2.1 Three-address machines	34
	3.2.2 Two-address machines	37
	3.2.3 One-address machines (Accumulator machines)	
	3.2.4 Zero-address machines (Stack machines)	
	3.3 Register or memory?	42
	3.4 Problems in instruction set design	
	3.4.1 Operations in the instruction set	47
4. /	Addressing Modes	55
	4.1 Interpreting memory addresses	
	4.2 A classification of addressing modes	
	4.3 Immediate addressing	
	4.4 Displacement addressing	
	4.5 Indirect addressing (memory indirect)	
	4.6 Indexed addressing	
5 (CPU Implementation	75
<i>J</i> . C	5.1 Defining an instruction set	
	5.2 The instruction set.	
	5.3 Executing an instruction	
	5.4 Hardwired control	
	5.5 Performance for Hardwired Control	
6. I	Interrupts	
	6.1 Examples and alternate names	
	6.2 A classification of interrupts	
	6.3 Checking for interrupts	111
	6.4 Some problems in checking for interrupts	
	6.5 What is really hard about interrupts	
	6.6 A case study: interrupts in MIPS	118

7. The Memory Hierarchy (1).	123
7.1 The principle of locality	124
7.2 Finite memory latency and performance.	
7.3 Some definitions	127
7.4 Defining the performance for a memory hierarchy	129
7.5 Hardware/Software support for a memory hierarchy.	
7.6 How does data migrate between the hierarchy's levels	133
8. The Memory Hierarchy (2): The Cache	
8.1 Some values	
8.2 Placing a block in the cache.	136
8.3 Finding a block in the cache	138
8.4 Replacing policies.	145
8.5 Cache write policies.	149
8.6 The cache performance	
8.7 Sources for cache misses	
8.8 Unified caches or instruction/data only?	
9. The Memory Hierarchy (3): Main Memory	157
9.1 DRAM/SRAM	157
9.2 Possible organizations for main memory.	161
10. Virtual Memory	169
10.1 Some definitions	
10.2 How virtual memory works.	175
10.3 More about TLB	178
10.4 Problems in selecting a page size.	